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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04N 3/15 — A1

(11) International Publication Number: WO 99/05853

(43) International Publication Date: 4 February 1999 (04.02.99)

(21) International Application Number: PCT/US98/15144

(22) International Filing Date: 24 July 1998 (24.07.98)

(30) Priority Data:
08/899,560 24 July 1997 (24.07.97) US

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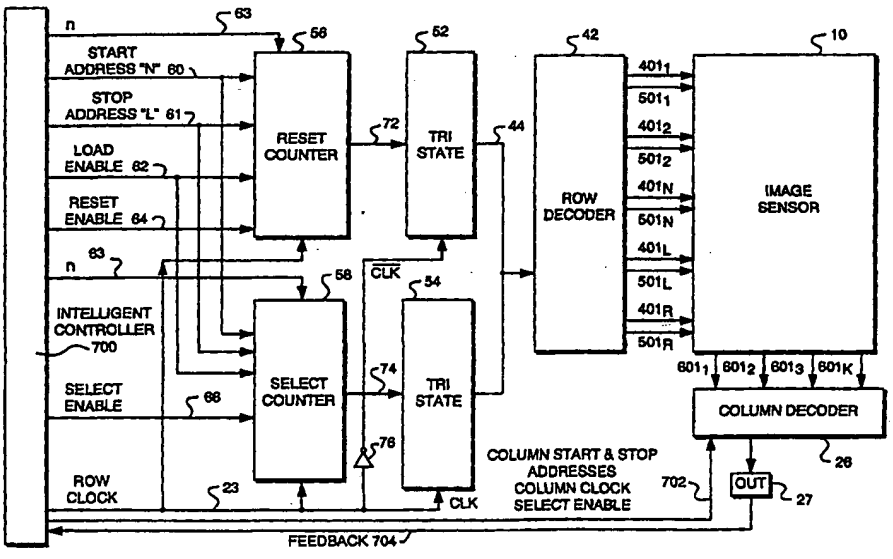
(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: FOCAL PLANE EXPOSURE CONTROL SYSTEM FOR CMOS AREA IMAGE SENSORS



(57) Abstract

An electronic exposure control system for an active pixel CMOS image sensor includes a row decoder and a column decoder for respective row–wise and column–wise addressing of the image signal generating pixels. The decoders receive row and column addresses and control signals from a controller. The row addresses received by the row decoder are alternately switched between a predetermined row address for resetting the image signals of pixels in said row and another predetermined spaced apart row address for enabling the image signals of pixels in said selected row to be read out by the column decoder. By providing a predetermined sequence of row addresses, a "rolling shutter" can be created and/or the exposure time of the pixels can be selected to be different from the time to expose an entire frame. The image sensor can also be operated in an interlaced mode and/or specific areas on the image sensor can be selected to be reset and read out.

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TITLE: FOCAL PLANE EXPOSURE CONTROL SYSTEM FOR CMOS AREA IMAGE SENSORS

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to an electronic exposure control system for a solid state image sensor, in particular for active pixel MOS image sensor (CMOS), and a method for using the same. More particularly, the invention relates to a "rolling readout" for the CMOS image sensor using row decoders wherein the pixel exposure time is different from the frame time and rows can be read out non-sequentially, one row at a time.

Background of the Invention

The present state of the art discloses at least two types of solid state image sensors used for image acquisition — charge coupled device (CCD) image sensors and complementary metal-oxide semiconductor (CMOS) image sensors. Although CCD image sensors have found wide-spread applications, for example in electronic video and still cameras, the process used in CCD fabrication is specialized and different from the process used for manufacturing other commonly used integrated electronic circuits (IC) employing MOS technology, such as microprocessors.

The individual radiation-sensing elements (pixels) in a CMOS array are basically reverse-biased semiconductor junctions of the type normally used to form source and drain regions of MOS transistors. Radiation is sensed by: i) applying a large reverse bias to the device (a reset signal), ii) isolating the device from the reverse bias voltage, and iii) measuring the decrease in the charge stored in the reverse-bias junction capacitance of the device by either sensing the reverse-bias potential (i.e., voltage-mediated sensing or read-out) or by integrating the reverse-bias current flowing through the device (i.e., current-mediated sensing or read-out). The reset function can also be executed by either a voltage source or a current source. The features of a current-mediated active-pixel image sensing device are described in detail in U.S. Application Serial No. 08/595,981 by McGrath et al., entitled "Current-mediated active-pixel image

sensing device with current reset" which is assigned to the same assignee as the present invention and which is incorporated herein by reference.

Electronic image sensors have a defined exposure range, not unlike conventional film. If the exposure time is too short, for example, almost no charge is drained from the reverse-biased junction and the resulting small voltage drop is very small and difficult to measure. Consequently, a large noise-to-signal ratio results. If the exposure time is too long, almost all pixel charge may be drained and little image content or image contrast will result. A shutter is provided for providing proper exposure of the pixels to incoming radiation. The shutter may be mechanical, such as the shutter in a photographic camera using film, as described, for example, in U.S. Patent 5,341,220. Alternatively, the shutter may be electronic, such as comprising a variable pre-amplifier to control the time between reset and read-out of pixels as a function of the intensity of the incoming radiation.

An electronic shutter for a linear CCD array is described, for example, in U.S. Patent 5,303,052 wherein a shutter timing unit generates a shutter pulse between read-out pulses for draining excess charge accumulated in the CCD pixels. A similar concept for CCD video area image sensors is described in U.S. Patent 5,247,367 in which the shutter speed is controlled by adaptively varying the duration of light storage of the CCD for every vertical frame period in response to the radiative intensity.

The pixel signals of CMOS image sensors are typically read out in a different manner than read out performed with CCD image sensors. All pixels in each row are commonly addressed by digital circuitry one row at a time, such as in a shift register, either to be reset or to be selected for read out. When a row is enabled for read out, columns are sequentially selected and the signal of the pixel at a commonly selected row and column is read out by a charge sense amplifiers connected to the column lines. Such a read-out method is described, for example, in U.S. Patent 5,345,266. In many cases, shift registers are used in the digital circuitry for row (and also column addressing). Shift register addressing allows simple operation of the sensor. Addressing a row requires placing a "one" at the input of the shift register and then shifting the appropriate number of rows.

It is possible to provide with row addressing via a shift register, a pixel exposure time which is shorter than the frame time. This is accomplished by resetting a first row at the beginning of a frame using a first shift register, by then consecutively resetting succeeding rows, one row at a time, with the first shift register, and by reading the first row at a later time which is less than the frame time, using a second shift register which is delayed with respect to the first shift register by a certain number of rows which is less than the number of rows in the frame. A shutter of this type is described, for example, in U.S. Patent 5,410,348, using two row shift registers. Shift registers, however, are disadvantageous in that once the read-out time has been set by specifying the delay time between the two shift registers, this delay time cannot be changed at a later time unless the shift registers are reset to their start address, making it difficult to read out partial frames and to dynamically adapt the "electronic exposure time" to changing illumination conditions.

The disadvantages of the method described above can be obviated by employing decoders instead of shift registers. With decoder addressing, a specific row is selected by placing a word at the input to the decoder. One word is required per horizontal or per vertical direction. Decoder addressing requires more I/O but is more versatile. Regions of interest can be read out as well as various other non-sequential read-out schemes for exposure control can be envisioned.

SUMMARY OF THE INVENTION

With the foregoing in mind, it is therefore an object of the invention to provide an improved control system for controlling the exposure of pixels of a CMOS image sensor to incident optical radiation. The specification discloses a CMOS image sensor having two input lines per row — a first row input line for resetting and a second row input line for selecting pixels in one row to be read out by a column decoder, in parallel to respective output terminals of a row decoder. The input of the row decoder is connected to a reset and a select counter, respectively, via respective buffer amplifiers. The reset counter and the select counter, respectively, are connected to an "intelligent" controller to receive input signals from the output of the controller. The input signals include row clock pulses, start and stop addresses of the rows defining the row-wise imaging area, respective reset enable pulses and select enable pulses, a load enable pulse for loading the start and stop addresses into the respective counters and a preset incremental value for the row count. The select enable pulse is delayed with respect to the reset enable pulse by a certain number of row clock cycles defining the "height" of the rolling focal plane shutter and thus the respective pixel integration time.

The input signals received by the reset counter and the select counter, respectively, include the row addresses and the reset and select enabling signals; these addresses and enabling signals are alternately switched during one row clock cycle by the respective buffer amplifier. Pixels in columns can be addressed and the signals stored therein can be read out by a column decoder, which can also be controlled by the "intelligent" controller. The exposure information contained in the pixels can also be used to modify the output signals supplied by the "intelligent" controller. Both the exposure time of pixels and the area of the image sensor addressed for reset and readout can thus be changed in response to the image content.

A fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The structure and operation of the invention, together with other objects and advantages thereof, may best be understood by reading the detailed description to follow in connection with the drawings in which unique reference numerals have been used throughout for each part and wherein:

Fig. 1 a schematic block diagram of a CMOS image sensor with conventional shift register addressing for row-wise pixel reset and readout;

Fig. 2 a schematic block diagram of an exposure control system of the invention;

Fig. 3 a flow diagram for an exposure control system of the invention; and

Fig. 4 the CMOS imager of Fig. 2 depicting four representative pixels.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Fig. 1, there is shown a schematic block diagram of a CMOS image sensor 10 addressed in a conventional manner by shift registers 12, 14. CMOS image sensor 10 comprises pixels 31_1, 31_2, 31_3,...31_K arranged in R rows and K columns (for clarity, only representative pixels in the first row are shown, with the index K denoting the last column). Each pixel 31_i in a particular row is connected to a corresponding row select line 101_1,101_2, ..., 101_N, ..., 101_L, ..., 101_R for enabling readout of information stored in pixel 31_i, and is connected to a common row reset line 201_i for resetting all pixels in row i. A CMOS image sensor of this type is, for example, described the above-referenced U.S. Patent Application Serial No. 08/595,981. There is provided a select shift register 12 having R logical outputs, each logical output connected to one of row select lines 101_1,101_2, ..., 101_N, ..., 101_L, ..., 101_R for enabling the respective row of pixels 31_i to be read pixel-wise by a column shift register 16, with the image information provided at an output 17. There is also provided a reset shift register 14 also having R logical outputs, each of which is connected to one of row reset lines 201_1, 201_2, ..., 201_N, ..., 201_L, ..., 201_R for resetting one row of pixels. The inputs of both select shift register 12 and reset shift register 14 are connected to clocks 22, 25, respectively, for receiving row clock pulses via row clock input lines 20, 24, respectively. The output of column shift register 16 is connected in parallel to the column inputs of CMOS image sensor 10 via column enable lines 301_1, 301_2, 301_3, ..., 309_K, with one column enable line for each column. The signal readout lines, one readout line associated with each column enable line, for reading the signal information generated by the pixels in response to exposure to optical radiation and supplied to output 17, are not shown. Shift registers of this type and the use thereof for addressing image sensor arrays are known in the art and will not be discussed here in detail. Also not shown are the reset inputs for resetting and addressing each of the shift registers 12, 14, 16.

During operation of CMOS image sensor 10, a specific row N is read out M row clock cycles after the row L is reset. Row L is spaced apart M rows from row N. In the present example, row L is reset by applying a logical signal to reset line 201_L. Row N

is enabled for readout by applying a logical signal to select line 101_N. During operation, reset shift register 14 is enabled by receiving a logical signal at input 19, by which row reset line 201_1 resets the first row of image sensor 10. During subsequent row clock pulses, reset line 201_2 resets the pixels in row 2, etc., until row M is reset via rest line 201_M. At this point, select shift register 12 is enabled by a logical signal at input line 18 and begins counting. Row select line 101_1 enables row 1 for readout. When row 1 is enabled, the pixels in the first row are sequentially enabled for read-out by column shift register 16 via column select lines 301_1, 301_2,... , 301_3, ..., 309_K. Read out is accomplished out via the associated column signal lines in a manner known in the art, thereby providing an image signal at output 17. Hereafter, the row following row 201_{M+1} is reset and the second row is enabled by select line 101_2 and read out. This is a continuous process, that is, the row which is read out is spaced apart M rows from the row which is reset. The value of M is usually less than the number N of rows in image sensor 10. This readout method will hereinafter be referred to as "rolling readout." After the last row is reset, the process can either be terminated or "wrapped around" to start anew with row 1.

One disadvantage of shift registers is the need to reset to "one," that is, the count is restarted at row 1. Consequently, it is generally difficult to read out partial frames and the readout time cannot be shorter than the frame time. Furthermore, shift registers have to be reset to the start position "one," if the value M is to be changed, (such as in response to changing illumination conditions).

It is known in the art to substitute decoders for shift registers. At the input, the decoder may receive a word address encoded in binary, hexadecimal or similar notation, and is capable of addressing separate output lines, with each output line corresponding to a different word address and/or a combination of a word address and other logical input signals. Decoders can be fabricated on the same chip and by the same process as the CMOS image sensor. Consequently, decoder addressing provides a significantly enhanced addressing functionality.

There is shown in Fig. 2 a control system 100, in accordance with the present invention, comprising a column decoder 26 and a row decoder 42 rather than shift registers as in the embodiment of Fig. 1. Each row of the R rows of pixels of image

sensor 10 is connected to row decoder 42 via a pair of row signal lines (e.g., the first row of pixels is connected to row signal lines 401_1 and 501_1). Control system 100 thus comprises ($2 \times R$) row signal lines. Of the row signal lines provided by row decoder 42, row signal line 401_i is connected to the select enable line of the *i*th row of CMOS image sensor 10 and row signal line 501_i is connected to the reset enable line of the same row of CMOS image sensor 10. For example, first row signal line 401_1 is connected to the select enable line of the first row, and row signal line 501_1 is connected to the reset enable line of the first row of the CMOS image sensor 10. Row decoder 42 thus provides logical select enable signals via row select lines 401_1, 401_2, ..., 401_N, ..., 401_L, ..., 409_R and provides logical reset signals via row reset lines 501_1, 501_2, ..., 501_N, ..., 501_L, ..., 509_R. These signals are supplied to the R rows of pixels of CMOS image sensor 10.

Logical reset signals received at the input of row decoder 42 are generated by a reset counter 56, and logical select signals received at the input of row decoder 42 are generated by a select counter 58. The functions of reset counter 56 and select counter 58 are controlled by an "intelligent" controller 700. As seen from the figure, controller 700 generates the following signals: i) a START ADDRESS 60 for identifying the first row of the CMOS image sensor 10 to be addressed, ii) a STOP ADDRESS 61 for identifying the last row of the CMOS image sensor 10 to be addressed, iii) a LOAD ENABLE signal 62 for loading the START and STOP addresses into respective registers in the respective counters 56, 58, and iv) RESET ENABLE 64, v) SELECT ENABLE signals 66, and vi) an optional row increment value n, at input 63, specifying the value by which the respective counters 56, 58 are incremented at each row clock cycle of a clock 23 (e.g. by 1 to sequentially address each row, by 2 to address every other row).

When RESET ENABLE signal 64 is set to "HIGH" (i.e. a logical 1), then reset counter 56 is enabled and increments the reset address via signal lines 72. When SELECT ENABLE signal 66 is set to "HIGH", then select counter 58 is enabled and increments the select address via signal lines 74. The input signals to reset counter 56 and select counter 58, (i.e. START ADDRESS 60, STOP ADDRESS 61, LOAD ENABLE 62, RESET ENABLE 64 and SELECT ENABLE 66, and clock pulses 23),

which are supplied by controller 700, can be implemented by hardware or software residing in controller 700, or provided by means of an external computer (not shown).

The output of reset counter 56 and select counter 58 are transmitted, together with the respective RESET ENABLE signal 64 or SELECT ENABLE signal 66, to an associated set of tri-state buffer amplifiers 52 and 54 via signal lines 72 and 74, respectively, to the input of row decoder 42 via signal bundle line 44. Tri-state buffer amplifiers 52 and 54 are generally designed to provide three different output states: i) a first low-impedance output state providing a logical 0, ii) a second low-impedance output state providing a logical 1, and, iii) a third high-impedance output state. In the present embodiment, switching between the low impedance output state and the high impedance output state in tri-state buffer amplifiers 52, 54 is accomplished by row clock signal 23. When row clock signal 23 is "HIGH" (CLK), then both tri-state buffer amplifiers 54 are "conductive", and supply the word address and SELECT ENABLE signal 66 received from select counter 58 to row decoder 42. At the same time, an inverted clock signal is supplied to both tri-state buffer amplifiers 52, which are now "open" and have an infinitely high output impedance. Consequently, the output signal supplied by tri-state buffer amplifiers 54 on a common row address line 44c of signal bundle line 44 (see Fig. 4) is not affected. Conversely, during the next half clock cycle, CLK goes to "LOW" and the foregoing states invert. $\overline{CLK}$ is now "HIGH" and tri-state buffer amplifiers 52 are "conductive", thus supplying the word address and RESET ENABLE signal 64 received from reset counter 56 to row decoder 42. Tri-state buffer amplifiers 52 are now "open." As a result, row decoder 42 receives, alternately (depending on the clock cycle), signals comprising a respective word addresses of a specific row in conjunction with either logical RESET ENABLE signal 64 or SELECT ENABLE signal 66.

In the manner of an example, if the row (word) address at the output of reset counter 56 is "L" and the row (word) address at the output of select counter 58 is "N", and if both RESET ENABLE signal 64 and SELECT ENABLE signal 66 are "HIGH", then select line 401_N will be asserted (i.e. set to a logical 1 or "HIGH") on CLK and reset line 501_L will be asserted on $\overline{CLK}$. If one or both of SELECT ENABLE signal

66and RESET ENABLE signal 64 are "LOW", then the respective select or reset lines 401_N and 501_L will not be asserted.

There is shown in Fig. 3 a flow diagram 800 by which the method for addressing CMOS image sensor 10 can be explained in greater detail. For clarity of illustration, n has been set equal to 1. In step 810, START address word 60 ("N"), STOP address word 61 ("L"), the "height" of the rolling focal plane shutter expressed as number of rows ("M"), and row increment value n are provided along with CLK signal 23. In step 812, the addresses are loaded into reset counter 56 at step 814, and simultaneously into select counter 58, at step 834. Both reset counter 56 and select counter 58 begin counting upward from START address 60 to STOP address 61 after RESET ENABLE signal 64 and SELECT ENABLE signal 66 have been set to "HIGH". With START address "N" loaded into reset counter 56, RESET ENABLE 64 is set to "HIGH".

Since RESET ENABLE, in step 816, is "HIGH", row "N" is reset in step 818 during the negative-going clock signal $\overline{CLK}$ and the row number is incremented by n after reset. In branch point 820, the reset row address is checked to determine if it is less than or equal to (N+M). That is, whether the last row in the presently defined rolling focal plane shutter window has been reset. If the reset row address is less than or equal to (N+M), then it is checked at branch point 822 if the row address last reset is less than or equal to "L" (i.e. the STOP address 61). If this is the case, then the process will loop back to step 818 on the next row clock cycle. If the last row "L" has been reset, then from step 822 the process branches to step 824 where RESET ENABLE 62 is set to "LOW". A waiting period is introduced in step 826 if the illumination level is too low and it is thus necessary that the shutter be kept open longer than the frame time for proper exposure. In this case, the pixels in rows between "N" and "L" can be exposed to the radiation for longer than the frame time.

If the row address following the previous row address reset in step 820 is greater than (N+M),that is, the entire "height" of the rolling focal plane shutter has been reset, then the first row "N" in the frame will be read out during the next positive row clock pulse CLK. This is accomplished by branching from step 820 to step 828, where SELECT ENABLE 66 is set to "HIGH".

After step 826 or, alternately, if the reset row address in step 820 is larger than (N+M), then SELECT ENABLE 66 is set to "HIGH" in step 828 and the pixel data in row "N" are read out in step 842 during the positive row clock signal CLK supplied by row clock 23. The function of step 840 is to increment the row address of the select counter 58 only in the event that SELECT ENABLE 66 is "HIGH". After row "N" has been read out by column decoder 26 in step 842, the row address in select counter 58 is incremented by n (which is equal to one in this example). After the final row "L" has been selected and read out, step 844 branches to step 846 where SELECT ENABLE 66 is set to "LOW" and new addresses are loaded, or the previous addresses are reloaded into reset counter 56 and select counter 58. Alternately, if the select row address is less than or equal to "L", i.e. the last row of the rolling focal plane shutter has been read out without reaching the STOP ADDRESS "L" of the frame, then the process branches to the input of step 816. At this point, both RESET ENABLE 64 and SELECT ENABLE 66 are "HIGH", and the process described above repeats until all rows inside the defined frame have been reset and subsequently read out.

In the present embodiment, the same START address 60 and STOP address 61 ("N" and "L", respectively) are provided to the input of both reset counter 56 and select counter 58. "N" can be any number between 1 and the maximum number of rows, R, of CMOS image sensor 10. Similarly, STOP ADDRESS 61 "L" can be any number greater than N and smaller than the maximum number of rows, R, of the CMOS image sensor 10. START address 60 and STOP address 61 may be loaded asynchronously. The waiting time in step 826 can be computed in known ways by controller 700 from the output values at output 27.

As can be seen from Figs. 2 and 3, the time elapsing between resetting a certain row N and reading out that same row N through column decoder 26 is M row clock cycles, unless a waiting time is introduced. Row clock rates for an imager having 780 rows are typically on the order of 1 to 10 MHz, but may also be higher or lower, depending on the desired operating environment. Consequently, the effective exposure time of the CMOS image sensor 10 can be advantageously adjusted by simply adjusting the number of clock cycles between RESET ENABLE 64 and SELECT ENABLE 66 signals. For example, for a high illumination level, the value of M would preferably be

small; for a low illumination level, the value of M would be a larger value, preferably less than or equal to the total number of rows, R, of CMOS image sensor 10.

It is evident from the foregoing that the disclosed rolling focal plane exposure control system can also be used for reading a specific image area located within the image sensor area, that is, a partial frame. For example, if a vertical area in the center of the image sensor 10 extending over 1/3 of the total image sensor height is to be read, then $N = \frac{R}{3}, L = \frac{2R}{3}$ where M can be any number less than $\frac{R}{3}$. A horizontal area extending over the partial width of the image sensor can be selected in a similar fashion by addressing the column decoder 26 accordingly.

Another advantage is that the disclosed control system can capture and read out a scene having a low illumination level requiring an exposure time which is longer than the frame time. This is accomplished by adding a waiting time so as to modify the input parameters supplied by controller 700. The waiting time may be implemented either by not supplying the row clock pulses to reset counter 56 and select counter 58 during this time, or by setting reset enable 64 to "LOW". During the waiting time, the charge stored in the pixels of image sensor 10 changes. In this way, an arbitrarily long integration time can be achieved, limited only by other parameters of the image sensor, such as noise.

Advantageously, output 27 containing exposure information can be fed back to controller 700 via feedback line 704 and used to adjust START 60 and STOP 61 addresses to change the image size and/or to adjust the time delay between RESET ENABLE 64 and SELECT ENABLE 66 signals to change the height of the rolling focal plane shutter and thereby the pixel exposure time. Other features in certain regions of an image can also be monitored and adjusted for exposure time in this manner.

The invention can also advantageously be used for providing customized readout wherein, for example, a 512×768 pixel imager would be operated in a 256×384 pixel mode. This is accomplished by, for example, setting the increment value 63 to n = 2. Alternatively, CMOS image sensor 10 could be operated in an interlaced mode by setting increment value 63 to n = 2 and by toggling START address 60 "N" and STOP

address 61 "L" between two adjacent values after every $\frac{L-N}{2}$ row clock cycles in steps 848 and 810 of Fig. 3. It is also possible to address rows at random by loading different addresses after an arbitrary number of clock cycles.

The connections of the different signal lines to the row and column inputs to a section 10′ of CMOS image sensor 10 are shown in greater detail in Fig. 4. Pixels 10aA and 10bA in row A and columns a and b, respectively, are reset by sending the word "A" to input 44c of row decoder 42 while sending a logical "1" to reset input 44a. Inputs 44a, 44b and 44b form signal bundle line 44 (see Fig. 2). The output of row decoder 42 then provides the logical signal via row reset line 501_A for resetting the two pixels in row A. Column decoder 26 has no function during reset.

Pixel 10aA is selected for readout by sending the word "A" to input 44c of row decoder 42 while sending a logical "1" to select input 44b. In the case for readout, column a is selected in column decoder 26 by supplying the word "a" to input 701 of column decoder 26. Column decoder 26 then selects the pixels in column "a" via column select line 601_{a1}. The charge stored in pixel 10aA is then read out by the respective signal line 601_{a2} and supplied to output 27. The respective column select lines and column signal lines in Fig. 1 (denoted 301) and in Fig. 2 (denoted 601) are shown as a single line, for the sake of clarity, and not as separate lines as in Fig. 4. Lines 301 and 601, respectively, should however be understood to represent line pairs.

While there have been described what at present are considered to be the preferred embodiments of the present invention, it will be readily apparent to those skilled in the art that various changes may be made therein without departing from the spirit of the invention, and it is intended in the claims to cover such changes and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. A control system (100) for controlling the exposure of an active pixel image sensing device (10) having a plurality of image signal generating pixels (10aA) arranged in rows and columns to form a two-dimensional matrix, each row and column, respectively, having a respective row and column address, wherein the pixels in each row are connected to a common reset line (501) and a common select line (401), and the pixels in each column are connected to a common signal line (601), said control system (100) comprising:

row addressing means (42) connected to each of the reset lines (501) for resetting pixel image signals; said row addressing means (42) further connected to each of the select lines (401) for enabling the readout of pixel image signals;

column addressing means (26) connected to each of the signal lines (601) for reading out the signal of the pixel selected by the select line (401) and the signal line (601);

control means (700) connected to the row addressing means (42) for selecting a first and a second reset line, the second reset line spaced apart from the first reset line by a predetermined number of lines, for resetting the pixel image signals corresponding to the first reset line and for enabling the readout of the pixel image signals corresponding to the second reset line, said control means (700) further connected to said column addressing means (26) for selecting predetermined signal lines (601) to read out, in ordered sequence, pixel image signals from the row connected to the second select line, said control means (100) thereafter operating to control said row addressing means (42) for selecting predetermined ones of the reset lines and the select lines, and to control said column addressing means (26) for selecting predetermined ones of the signal lines (601) to read out pixel image signals from the rows connected to the selected select lines.

2. The control system of claim 1, wherein each succeeding one of the reset lines and select lines selected by said row addressing means is adjacent to the respective preceding selected one of the reset lines and to the respective preceding one of the select lines.

3. The control system of claim 1, wherein each succeeding one of the reset lines and select lines selected by said row addressing means is spaced apart by at least one row from the preceding selected one of the reset lines and select lines, respectively.

4. The control system of claim 1, wherein the row addresses supplied to said row addressing means by said control means comprise a row start address and a row stop address, with the rows located between said row start and row stop addresses defining a vertical frame.

5. The control system of claim 4, wherein the number of rows located between the row connected to the reset line and the spaced-apart row connected to the select lines is less than the number of rows in the frame and defines a shutter height.

6. The control system of claim 5, wherein said shutter height is changed by said control means in response to the image signals of the pixels received by said control means from said column addressing means.

7. The control system of claim 1, wherein said row addressing means comprises a decoder.

8. The control system of claim 1, wherein the image sensing device comprises a current-mediated active-pixel image sensing device.

9. A control system for controlling the exposure to incident optical radiation of an active pixel image sensing device having a plurality of image signal generating pixels arranged in horizontal rows and vertical columns to form of a two-dimensional matrix, each row and column, respectively, having a respective row and column address, wherein the pixels in each horizontal row are connected to a first common horizontal reset line and a second common horizontal select line and the pixels in each vertical column are connected to a common vertical signal line, the control system comprising:

a row decoder connected to each of said horizontal reset lines for resetting image signals of the pixels of a row connected to a predetermined first one of said horizontal reset lines; said row decoder also connected to each of said horizontal select lines for also selecting a predetermined one of said horizontal select lines for enabling image signals from pixels in the row connected to said second selected select line to be read out;

horizontal addressing means connected to each of said vertical signal lines for selecting a predetermined one of said vertical signal lines and for reading out the signal of the pixel simultaneously selected through said horizontal select lines and said vertical signal lines;

a control circuit for generating row and column addresses and control signals for controlling said row decoder and said horizontal addressing means;

two sets of tri-state buffer amplifiers, the input of each of the sets of tri-state buffer amplifiers connected to the output of the control circuit for receiving said row addresses and control signals from the control circuit, and the output of each of the sets of tri-state buffer amplifiers connected to the input of the row decoder for conveying said row addresses and control signals to the row decoder, each of said tri-state buffer amplifiers capable of switching between a low impedance output state and a high impedance output state in response to at least one of the control signals from the control circuit;

wherein said control device generates a first row address and a second row address and column addresses and respective control signals and conveys said first row address and

at least one of said respective control signals to a first one of said set of tri-state amplifiers and conveys said second row address at least one other of said respective control signals to a second one of said set of tri-state amplifiers, said row decoder receiving from the output of said first one of the sets of tri-state buffer amplifiers the first row address and the at least one respective control signal for selecting the horizontal reset line of that row having said first row address to reset the image signals of the pixels in that row having said first row address and thereafter receiving from the output of said second one of the sets of tri-state buffer amplifiers the second row address and said at least one other respective control signal for selecting the horizontal select line of that row having said second row address to enable the image signals of the pixels of that row having said second row address to be read out, wherein said second row address is spaced apart from said first row address by a predetermined number of rows, and said horizontal addressing means simultaneously selects in ordered sequence predetermined ones of said vertical signal lines to read out in said ordered sequence the image signals from the pixels of that row having said second row address,

said control device thereafter operating to generate succeeding predetermined new first and second row addresses and respective control signals to be alternately transmitted by said first and second set of tri-state amplifiers to the row decoder, and to control said horizontal addressing means to simultaneously select in ordered sequence predetermined ones of said vertical signal lines to read out in said ordered sequence the image signals from the pixels of the rows having said succeeding predetermined new second row addresses.

10. The control system of claim 9, wherein each succeeding predetermined new first row address and succeeding predetermined new second row address is the following next first and second row address, respectively.

11. A method for controlling the exposure to incident optical radiation of an active pixel image sensing device having a plurality of image signal generating pixels arranged in horizontal rows and vertical columns to form of a two-dimensional matrix, each row and column, respectively, having a respective row and column

address, the rows between the row start and stop address defining a vertical frame, wherein the pixels in each horizontal row are connected to a first common horizontal reset line and a second common horizontal select line and the pixels in each vertical column are connected to a common vertical signal line, the method comprising the steps of:

resetting the image signals of the pixels of a predetermined first row located within the vertical frame via the respective horizontal reset line of said predetermined first row;

thereafter selecting, via the respective horizontal select line, a predetermined second row spaced apart from said first row and located within said vertical frame for enabling image signals from pixels in the predetermined second row to be read out;

sequentially selecting columns in a predetermined order and reading out in said predetermined order the image signal of the pixel simultaneously selected in said predetermined second row and in said selected column;

selecting new predetermined first and second row addresses for said predetermined first row and said predetermined second row and repeating steps a) through d) at least until the image signals of the pixels of all rows in the frame are read out.

12. The method according to claim 11, wherein said the number of rows between said predetermined second row address and said predetermined first row address is less than the number of rows in the frame.

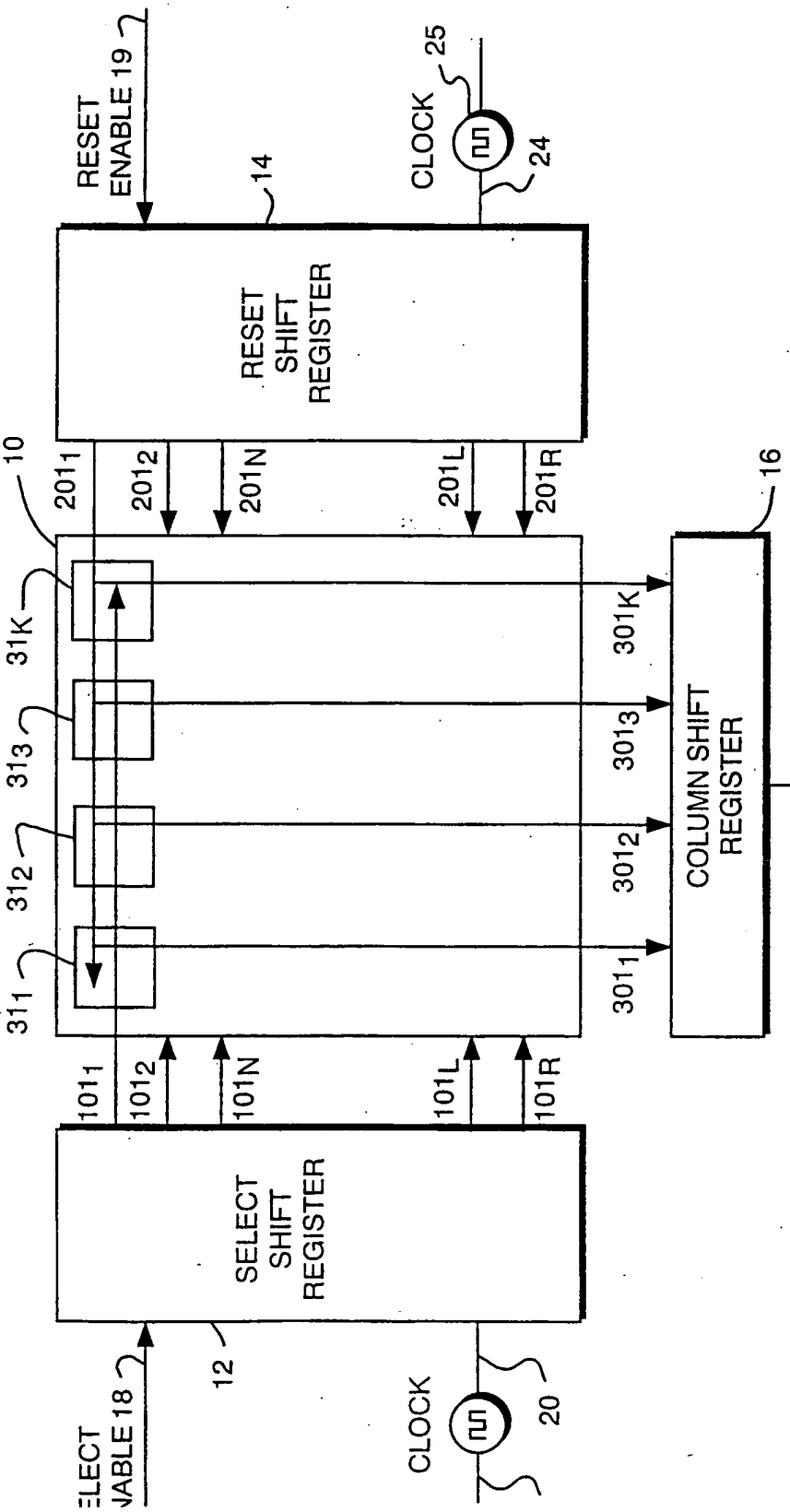


FIG. 1
(PRIOR ART)

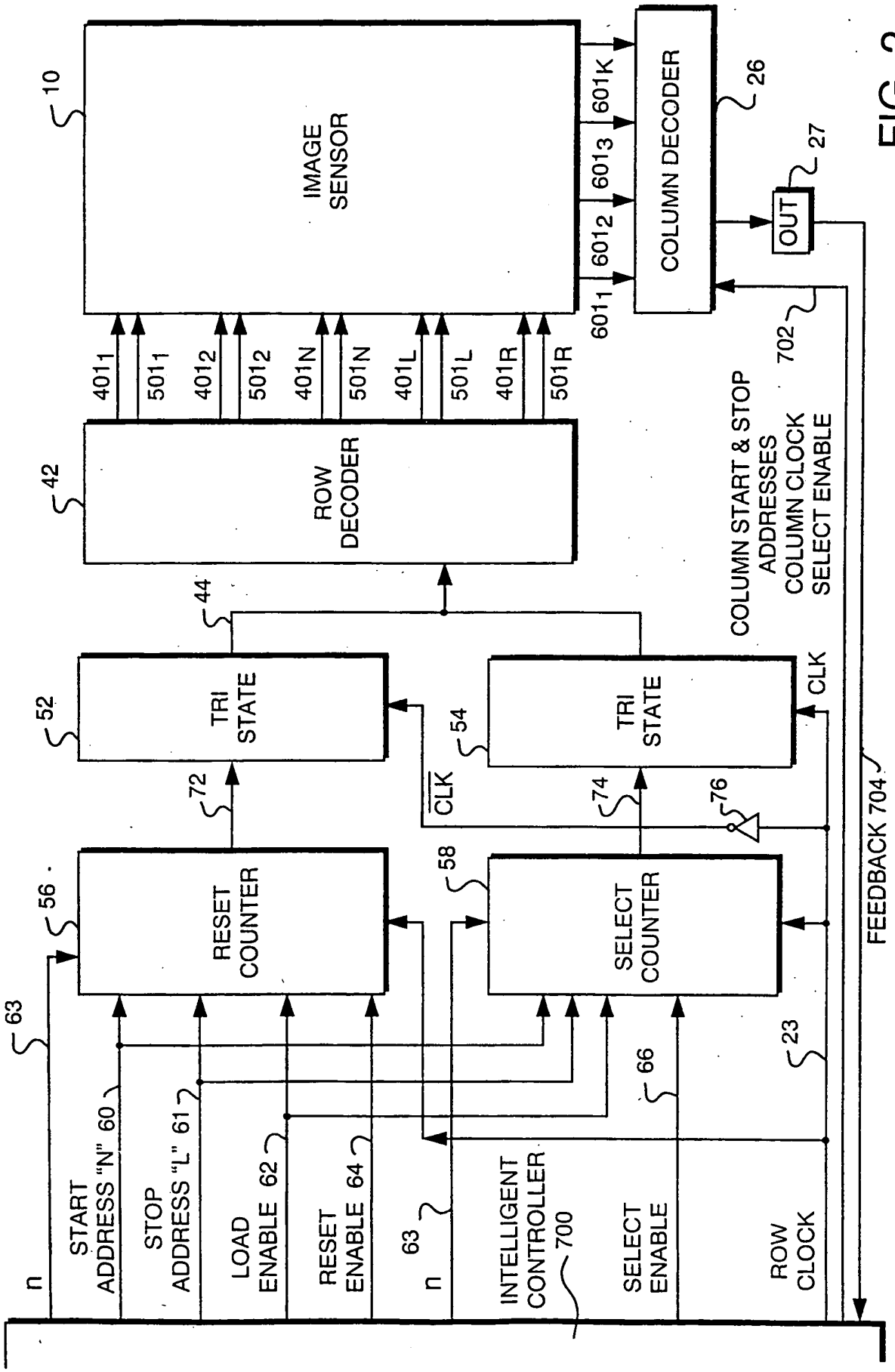
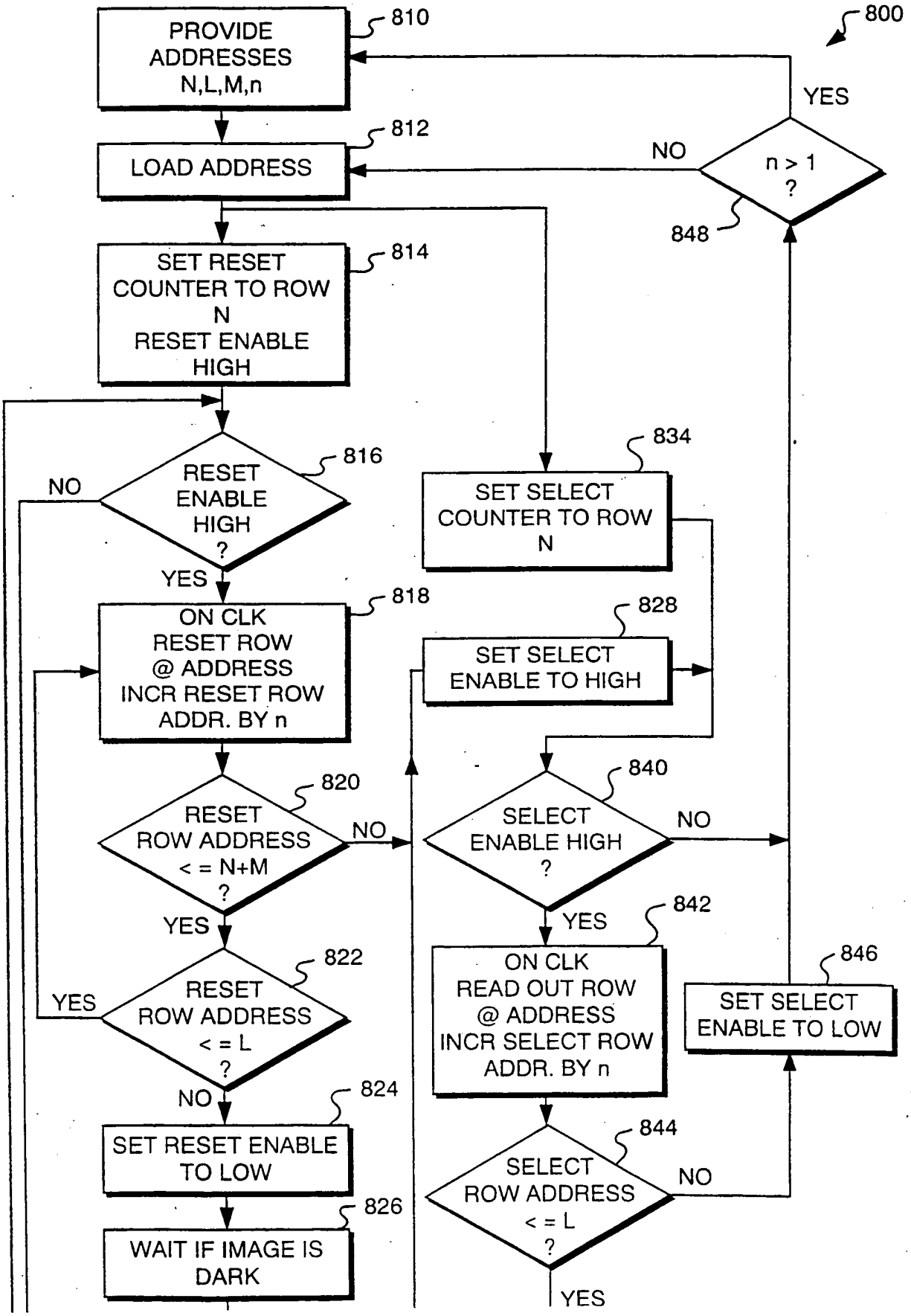

10
IMAGE SENSOR
26
COLUMN DECODER
27
OUT
601_1
601_2
601_3
601_K
42
ROW DECODER
401_1
501_1
401_2
501_2
401_N
501_N
401_L
501_L
401_R
501_R
44
52
TRI STATE
54
TRI STATE
CLK
$\overline{CLK}$
72
74
76
56
RESET COUNTER
58
SELECT COUNTER
63
n
START ADDRESS "N" 60
STOP ADDRESS "L" 61
LOAD ENABLE 62
RESET ENABLE 64
63
n
INTELLIGENT CONTROLLER 700
66
SELECT ENABLE
23
ROW CLOCK
FEEDBACK 704
702
COLUMN START & STOP ADDRESSES
COLUMN CLOCK
SELECT ENABLE

FIG. 2


800
PROVIDE ADDRESSES N,L,M,n
810
LOAD ADDRESS
812
SET RESET COUNTER TO ROW N
RESET ENABLE HIGH
814
RESET ENABLE HIGH ?
816
NO
YES
ON CLK RESET ROW @ ADDRESS INCR RESET ROW ADDR. BY n
818
RESET ROW ADDRESS < = N+M ?
820
NO
YES
RESET ROW ADDRESS < = L ?
822
YES
NO
SET RESET ENABLE TO LOW
824
WAIT IF IMAGE IS DARK
826
n > 1 ?
848
YES
NO
SET SELECT COUNTER TO ROW N
834
SET SELECT ENABLE TO HIGH
828
SELECT ENABLE HIGH ?
840
NO
YES
ON CLK READ OUT ROW @ ADDRESS INCR SELECT ROW ADDR. BY n
842
SELECT ROW ADDRESS < = L ?
844
NO
YES
SET SELECT ENABLE TO LOW
846

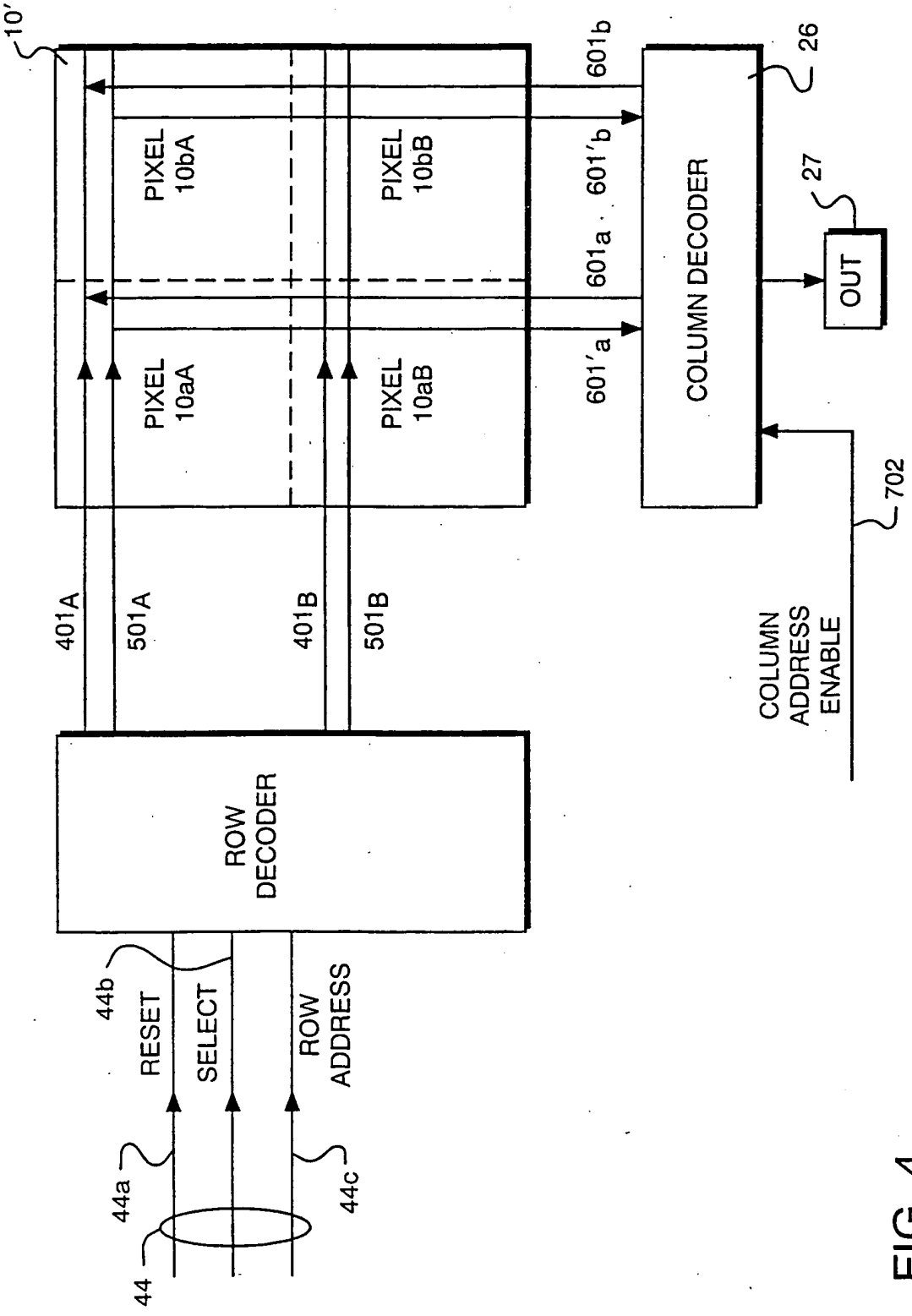

10'
PIXEL 10bA
PIXEL 10bB
PIXEL 10aA
PIXEL 10aB
601b
601'b
601a
601'a
26
COLUMN DECODER
27
OUT
702
COLUMN ADDRESS ENABLE
401A
501A
401B
501B
ROW DECODER
44b
RESET
SELECT
ROW ADDRESS
44a
44c
44

FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 98/15144

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 569 202 A (SONY CORP) 10 November 1993 see column 5, line 27 - column 7, line 10; figure 1	1,9,11
A	FR 2 538 651 A (THOMSON CSF) 29 June 1984 see page 4, line 8 - line 16; figure 1	1,9,11
A	US 5 262 871 A (WILDER JOSEPH ET AL) 16 November 1993 see column 4, line 54 - column 5, line 11; figure 1	1,9,11
A	US 5 410 348 A (HAMASAKI MASAHARU) 25 April 1995 cited in the application see column 4, line 1-59	1,9,11

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 September 1998	24/09/1998

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Ir ational Application No
PCT/US 98/15144

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	GOODENOUGH F: "GET READY FOR TV CAMERAS ON A CHIP" ELECTRONIC DESIGN, vol. 44, no. 4, 19 February 1996, page 125/126, 128 XP000580217 see page 128, left-hand column, line 22 - right-hand column, line 13 -----	1,9,11

INTERNATIONAL SEARCH REPORT

Information on patent family members

Ir ational Application No
PCT/US 98/15144

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		DE 69307947 D	20-03-1997
		DE 69307947 T	22-05-1997
		US 5420631 A	30-05-1995
FR 2538651 A	29-06-1984	EP 0117375 A	05-09-1984
		JP 59133780 A	01-08-1984
		US 4609825 A	02-09-1986
US 5262871 A	16-11-1993	NONE	
US 5410348 A	25-04-1995	JP 5227489 A	03-09-1993